A Compact and Low Phase Noise Square-Geometry Quad-Core Class-F VCO Using Parallel Inductor-Sharing Technique

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***Abstract*— This article introduces a compact and low phase noise (PN) 19-GHz quad-core class-F voltage-controlled oscillator (VCO) based on a square-geometry transformer tank using the inductor-sharing technique. The proposed square-geometry transformer tank is inherently more compact than the prevalent topologies such as star geometry, dual-row geometry, and circular geometry. The inductor-sharing technique is introduced to merge neighboring inductors into smaller ones, which further reduces the chip area. Moreover, the proposed quad-core topology supports impedance boosting at harmonic frequencies without extra chip area consumption and class-F operation is adopted to achieve better PN performance. The quad-core VCO prototype is designed and fabricated in a 65-nm CMOS process. Measured performances are 17.6 to 19.4 GHz frequency range with −137.2 dBc/Hz minimum PN at 10 MHz offset from 19 GHz carrier with 46 mW power consumption and 0.9-V supply, resulting a figure of merit (FoM) of 186.1 dBc/Hz. Thanks to the proposed square-geometry and inductor sharing technique, the proposed VCO is the smallest in quad-core VCOs with a similar operating frequency with a core chip area of 0.3 × 0.3 mm^2 and the corresponding FoM$_A$ is 196.5 dBc/Hz.**

***Index Terms*— Class-F oscillator, CMOS, multi-core oscillator, phase noise (PN), voltage-controlled oscillator (VCO).**

I. Introduction

THE rapid development of the next-generation high-speed wireless communication system has set increasingly stringent requirements on the spectral purity of local radio frequency (RF) oscillators. Advanced communication systems have data rates in the tens of Gbps, which will continue to grow in the future. Besides, they also promise increased network capacity and lower latency, which enables a new kind of network that is designed to connect virtually everyone and everything together including machines, objects, and devices. To support this high data rate and low latency wireless link, next-generation communication protocols resort to higher-order quadrature amplitude modulation (QAM), which mandates lower error vector magnitude (EVM) and thus set a tighter constraint on the phase noise (PN) of the frequency synthesizer. For example, as discussed in [1], for quadrature phase shift keying (QPSK), the PN at 1 MHz offset for 80 GHz carrier frequency needs to be less than −90 dBc/Hz to guarantee the 10^{-6} bit error rate (BER). For 64 QAM, the PN needs to be less than −102 dBc/Hz. The stringent requirement for millimeter-wave oscillators with lower PN is continuously driving voltage-controlled oscillator (VCO) circuit innovations.

PN in *LC* oscillators due to white noise at offset frequency $\Delta\omega$ is given by Leeson's equation [2]

$$\mathcal{L}(\Delta\omega) \propto \frac{2Fk_BT}{P}\left(\frac{\omega}{2Q\Delta\omega}\right)^2 \propto \frac{\omega^3 L}{A^2 Q} \tag{1}$$

where k_B is Boltzmann's constant, T is the absolute temperature. P is the average power dissipated in the resistive part of the tank, ω is the oscillation frequency, Q is the effective quality factor of the tank, F is the noise factor determined by the topology of the oscillator, accounting for the extra noise added by the active core. The equivalent resistance of the *LC* tank at the oscillation frequency is $R_P = \omega LQ$, where L is the tank inductance. Substitute P with A^2/R_P, A is the oscillation amplitude. For a given topology and oscillation frequency, to achieve low PN levels, one should scale down the inductance L while maintaining its quality factor Q. However, as the inductance reduces, the coupling between inner edges will increase and a Q drop-off occurs [3].

To circumvent the "small inductor" problem and further improve PN, a viable popular approach is to couple N identical oscillators with relatively large inductors together [1], [2], [3], [4], [5], [6]. The equivalent inductance is reduced by a factor of N, which ideally improves the PN by $10\log_{10}N$ at the cost of N times higher power consumption. Clearly, implementing N coupled oscillators comes with the drawback of area penalty and introduces additional design concerns. The design of the coupling network is not trivial. It should be as follows: 1) tightly synchronize the phase of each core against frequency mismatches due to PVT variation; 2) be able to effectively suppress undesired

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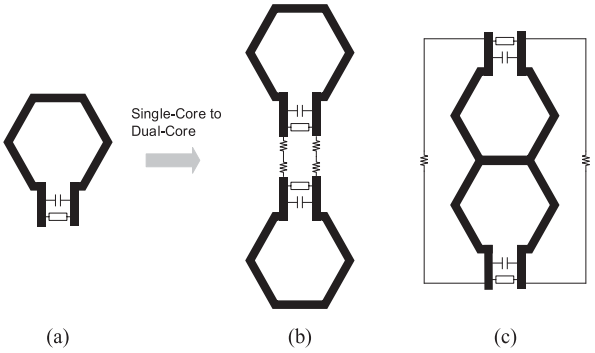


Fig. 1. Evolution from single core to dual core. (a) Single-core VCO. (b) Tail-to-tail dual core. (c) Head-to-head dual core.

multi-tone concurrent oscillations introduced by multi-core configuration; and 3) introduce less parasitics to the oscillators as possible. As N increases, the coupling network becomes even more difficult to design.

This article is organized as follows. Section II gives a brief review of the previously reported multi-core oscillators and compares various multi-core oscillator topologies. Section III describes the proposed multi-core architecture with inductor sharing technique and analyzes the mode ambiguity issues. Section IV discusses the detailed circuit implementation of the proposed quad-core VCO. Section V presents the measurement results of the 19-GHz prototype. Finally, conclusions are drawn in Section VI.

II. Brief Review of Multi-Core VCOs

The floorplan of the dual-core VCO is rather straightforward using a tail-to-tail [4], [5], [6], [7], [8], [9], [10] or a head-to-head [11], [12], [13], [14] topology. The tail-to-tail floorplan makes the outputs of the VCO cores very close to each other, as shown in Fig. 1(b). Thus, the in-phase terminals of the VCO cores can be connected through metal wire, which is equivalent to a small resistor [4]. In [5], the interconnecting wire is substituted by transistor switches. The VCO can be reconfigured to a single core to trade PN performance for power consumption when a low-power mode is preferred. In [6], [7], [8], [9], and [10], a switch-capacitor array is introduced to couple the VCO cores and select different oscillation modes. The reduction of PN and the extension of the tuning range are achieved simultaneously. The frequency tuning range is as wide as 42.3% in [9] and 73% in [7] and [8] where E-M mixed-coupling resonance boosting is applied. In the head-to-head floorplan [11], [12], [13], as shown in Fig. 1(c), the inductor shows a shape of figure "8," which greatly suppresses the EM interference from neighboring aggressors. In [13] uses a small metal resistor to resist unwanted modes of oscillation while [11], [12] adopt the switch-capacitor array to expand the frequency tuning range similar to [6], [7], [8], [9], and [10].

There are two popular topologies when a dual-core VCO is duplicated to quad-core, dual-row geometry as shown in Fig. 2(a), and star-geometry as shown in Fig. 2(b). For the star-geometry [1], [15], [16], [17], [18], the coupling network and the active devices of the VCO cores can be placed together,

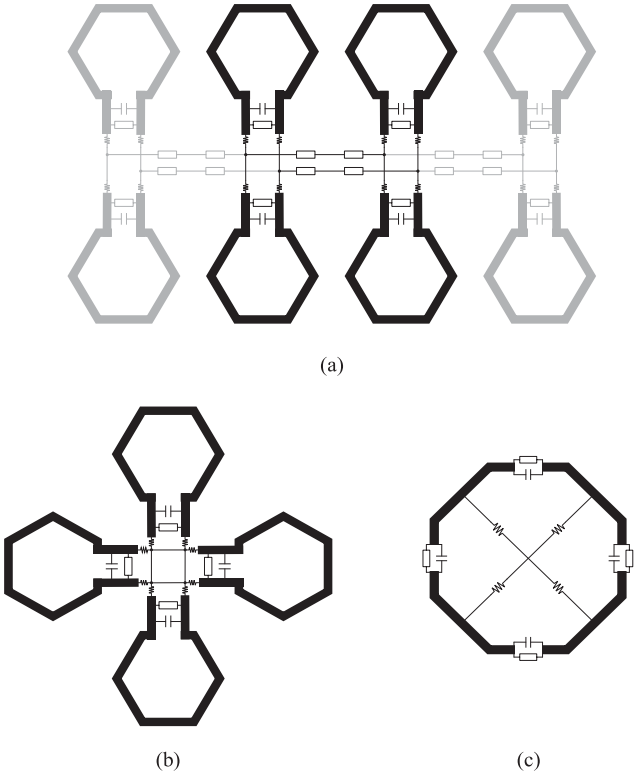


Fig. 2. Comparison of different topology multi-core oscillators. (a) Dual-row geometry. (b) Star geometry. (c) Circular geometry.

avoiding long connection wires. In addition, the layout is symmetric both horizontally and vertically which minimizes the mismatch between VCO cores. Similar to the dual-core VCOs, the global coupling is easy to implement in star-geometry quad-core VCO using small resistors [16], [17], transistor switches [1], [15], or switch-capacitor array [18]. However, the star-geometry is only suitable for quad-core VCO. If N increases further, this topology becomes no longer applicable. In [19] adopts ring connection but it also only supports quad-core because the layout will be complicated under the request of symmetry. In advanced CMOS technologies, all transistors are required to be aligned in the same direction, which makes the ring connection not suitable for multi-core VCOs with more than four cores. Another topology is dual-row geometry, as shown in Fig. 2(a). Two oscillators are coupled together tail-to-tail with low-ohmic lines same as Fig. 1(b) and form tightly coupled pairs, and all oscillators are arranged in two flipped rows. Clearly, the advantage of the dual-row geometry is that it is easy to expand beyond quad-core such as eight-core in [20], [21], and [22], and 16-core in [23]. Moreover, it is friendly to reconfigurable multi-core VCO by simply adding switches in the coupling network. Nevertheless, unlike star-geometry, it is difficult to implement global coupling in dual-row geometry multi-core VCO, because the active devices of all VCO cores are unlikely to be placed together so one may have to resort to the nearest neighbor bilateral coupling for this topology.

Both star geometry and dual-row geometry are area-consuming because they are simple N times duplication of single-core VCO. To mitigate the large chip area issue, circular

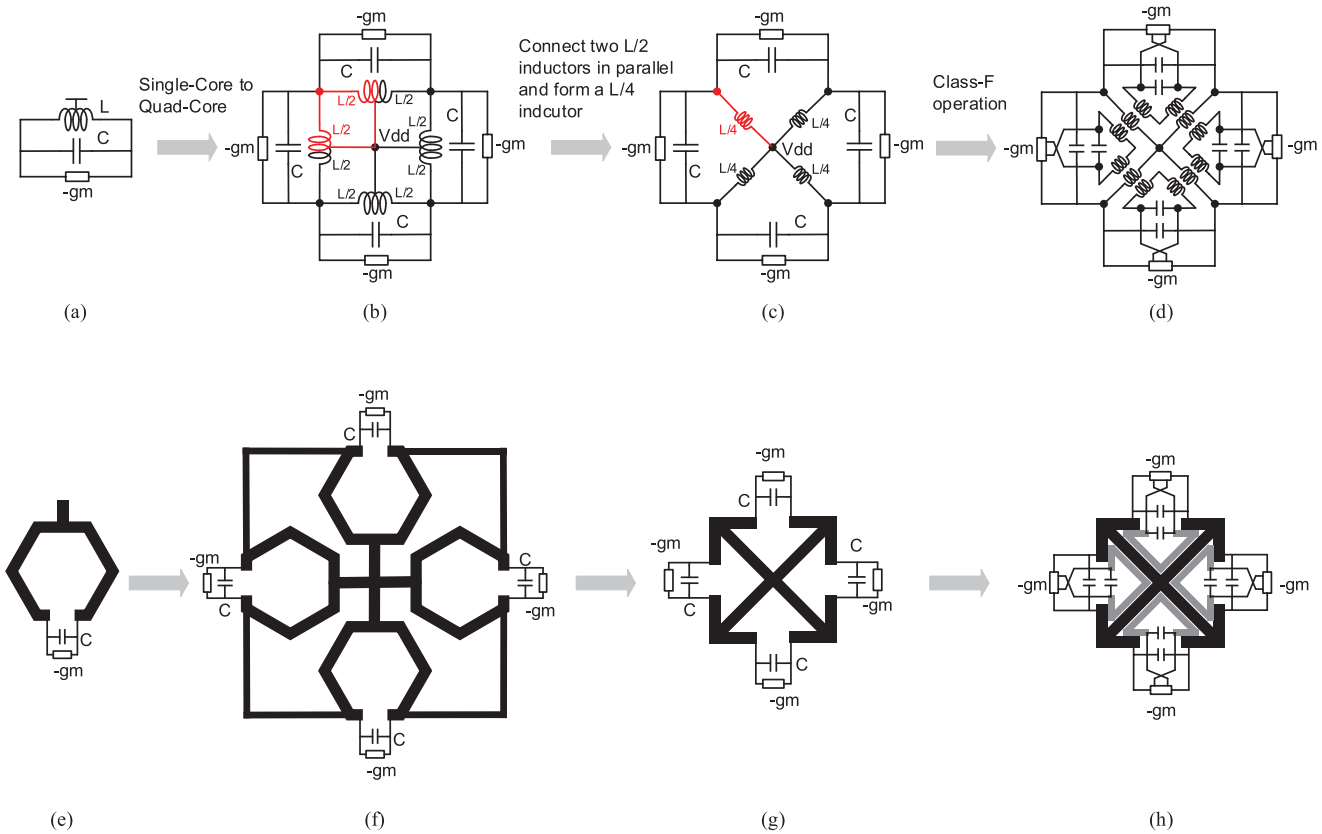


Fig. 3. Evolution from single-core to proposed square-geometry quad-core oscillator. (a)–(d) Schematic. (e)–(h) Layout.

geometry is proposed [3], [24], [25], [26], [27], [28], where the passives are merged into a single passive structure and the minimal realizable inductance is reduced while keeping a high Q-factor as shown in Fig. 2(c). The concurrent oscillation mode rejection is achieved by introducing losses into all unwanted modes to make sure only the loop gain of the desired mode is large enough to sustain oscillation. With an elaborate layout design, the quad-core ring topology can be expanded to 16-core [29]. However, this topology is only suitable for relatively high-frequency applications. When the frequency is relatively low such as the GHz range, the area-saving advantage is no longer obvious.

III. Square-Geometry Inductor Sharing Transformer Based Quad-Core VCO

This article proposes a different topology for multi-core VCOs called square-geometry, which has a very compact structure and greatly reduce the area occupation. Besides, based on the inductor sharing technique, the two inductors of adjacent VCO cores are merged together and turn into a smaller inductor and further reducing the chip area [30], [31]. In [30] brings up a conceptual model of coupled oscillators, where the coupling network is assumed to be ideal and the mode ambiguity issue is not considered. In addition, advanced oscillator techniques including harmonic shaping is not taken into consideration. Our work was first introduced in [31] and here we present more in-depth discussions with mode ambiguity rejection.

A. From Single Core to Multi-Core

The evolution of the schematic of the proposed circuit topology is depicted in Fig. 3(a)–(d) and the corresponding layout is shown in Fig. 3(e)–(h). A single-core VCO is represented by an LC tank paralleled with a negative resistor $-gm$ as shown in Fig. 3(a). With four identical VCO placed head-to-head and the outputs of adjacent cores connected together, a quad-core ring-topology VCO is constructed, as shown in Fig. 3(b). As can be seen from Fig. 3(f), the layout of the quad-core VCO is bulky and the chip area is even larger than four times of the single-core VCO depicted in Fig. 3(e) because there is a large vacancy at the four corners of the layout. This is where we introduce the inductor sharing technique and change the topology of quad-core VCO, which will greatly reduce chip area.

As shown in Fig. 3(b), the center tap of the inductors of four single-core VCOs are all connected to VDD and each inductor L can be split into two $L/2$ inductors. The two $L/2$ inductors of the adjacent cores are paralleled to each other and they can be merged into one inductor with an inductance of $L/4$, as shown in Fig. 3(c), and the topology of the quad-core VCO changes from a star-geometry to a square-geometry with the inductance reduced by four times, while keeping the frequency of the VCO unchanged. The layout of Fig. 3(c) is shown in Fig. 3(g), which is much more compact compared to Fig. 3(f). The square-geometry transformer also supports impedance boosting at harmonic

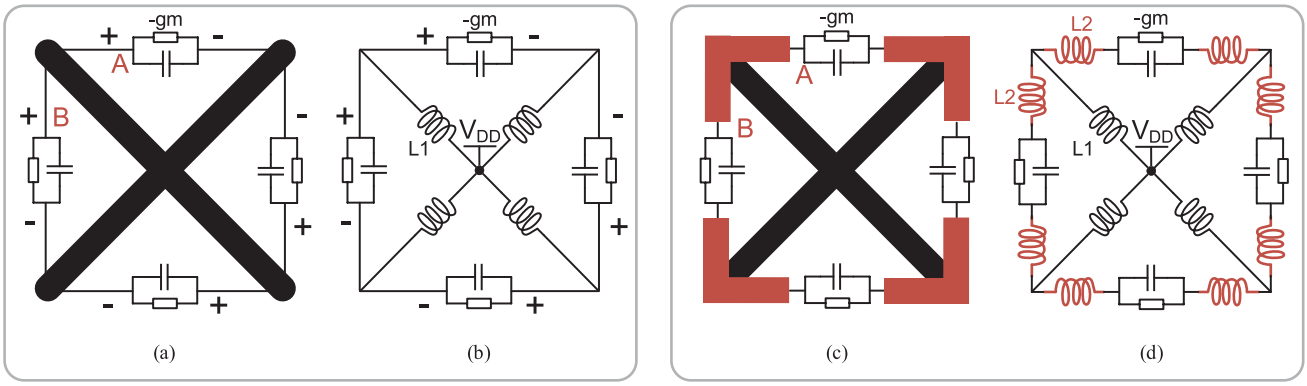


Fig. 4. (a) and (b) Layout and schematic of the ideal quad-core VCO without mode ambiguity. (c) and (d) practical quad-core VCO with non-negligible routing from inductor to active devices.

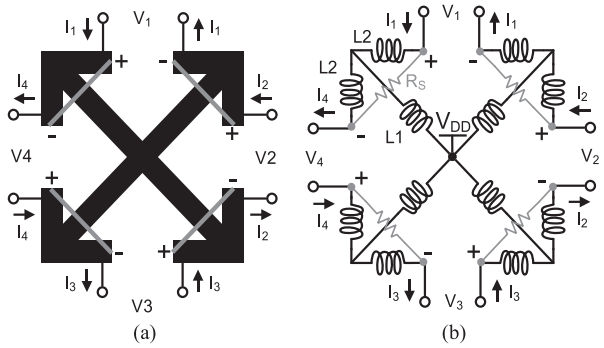


Fig. 5. (a) Proposed quad-core inductor with mode rejection resistor and (b) equivalent four-port model.

frequencies, therefore, has the potential to enable harmonic-shaping techniques that improve PN performance, such as tail filtering [32], [33], implicit common-mode resonance [34], [35], [36], and class-F operation [37], [38], [39]. In this article, in order to pursue lower PN performance, the class-F operation is achieved by adding a secondary winding coupled to the quad-core transformer as shown in Fig. 3(d) and (h) and it is worth mentioning that the introduction of class-F operation does not increase the size of the layout.

B. Inductor Sharing Technique

Ideally, the proposed quad-core square-geometry inductor should only route along the diagonal of the layout, as shown in Fig. 4(a) and (b). Under this presumption, the connection between the inductor and active devices is an ideal conductor wire. The negative resistance, usually implemented using cross-coupled differential pairs, forces the signal phase at its two ports to be opposite. As shown in Fig. 4(a) and (b), due to the ideal connection, point A and B always have the same phase, thus the quad-core VCO only has one oscillation pattern. However, in a practical layout, the routing from the inductor to active devices cannot be neglected because they are not very adjacent to each other. As shown in Fig. 4(c), the non-negligible routing is plotted using red wire and modeled as L_2 in Fig. 4(d). The signal phase at points A and B are not always the same and this will introduce mode ambiguity.

To suppress the unwanted mode, metal traces are introduced to connect the drain nodes of adjacent cores, as shown in Fig. 5(a). The narrow metal trace can be modeled as a resistor R_s as shown in Fig. 5(b). From the qualitative analysis, if the voltage across the two ports of R_s are in-phase, there will be no current flowing through the R_s, which will not degrade the Q-factor of the resonator. However, if the voltage across the two ports of R_s are out-of-phase, R_s will carry current, which degrades the Q-factor of the resonator and thus prevents these oscillation modes from happening.

To give a quantitative analysis, the proposed inductor is modeled as a four-port network with port voltage and current defined as Fig. 5(b). The four-port network can be represented by a 4×4 Z-matrix as follows:

$$Z = \begin{bmatrix} z_{11} & z_{12} & z_{13} & z_{14} \\ z_{21} & z_{22} & z_{23} & z_{24} \\ z_{31} & z_{32} & z_{33} & z_{34} \\ z_{41} & z_{42} & z_{43} & z_{44} \end{bmatrix} = \begin{bmatrix} a & b & c & b \\ b & a & b & c \\ c & b & a & b \\ b & c & b & a \end{bmatrix} \tag{2}$$

where the x and y plane symmetry of the network implies that

$$z_{11} = z_{22} = z_{33} = z_{44} = a \tag{3}$$

$$z_{12} = z_{21} = z_{23} = z_{32} = z_{34} = z_{43} = z_{14} = z_{41} = b \tag{4}$$

$$z_{13} = z_{31} = z_{24} = z_{42} = c. \tag{5}$$

The eigenvectors of Z are the normal oscillation modes and the eigenvalues of Z are the effective impedance of the system at oscillation. The eigenvalues of Z are given by

$$\begin{aligned} \lambda_1 &= a - 2b + c \\ \lambda_2 &= a + 2b + c \\ \lambda_3 &= \lambda_4 = a - c. \end{aligned} \tag{6}$$

Since the symmetry of the four-port structure, λ_3 and λ_4 are identical and only three distinct eigenvalues exist. The corresponding eigenvectors are given by

$$\begin{aligned} v_1 &= \begin{bmatrix} -1 & 1 & -1 & 1 \end{bmatrix}^T \\ v_2 &= \begin{bmatrix} 1 & 1 & 1 & 1 \end{bmatrix}^T \\ v_3 &= \begin{bmatrix} 0 & -1 & 0 & 1 \end{bmatrix}^T \\ v_4 &= \begin{bmatrix} -1 & 0 & 1 & 0 \end{bmatrix}^T. \end{aligned} \tag{7}$$

The four potential oscillation modes with current direction and magnetic field distribution are shown in Fig. 6(a)–(d),

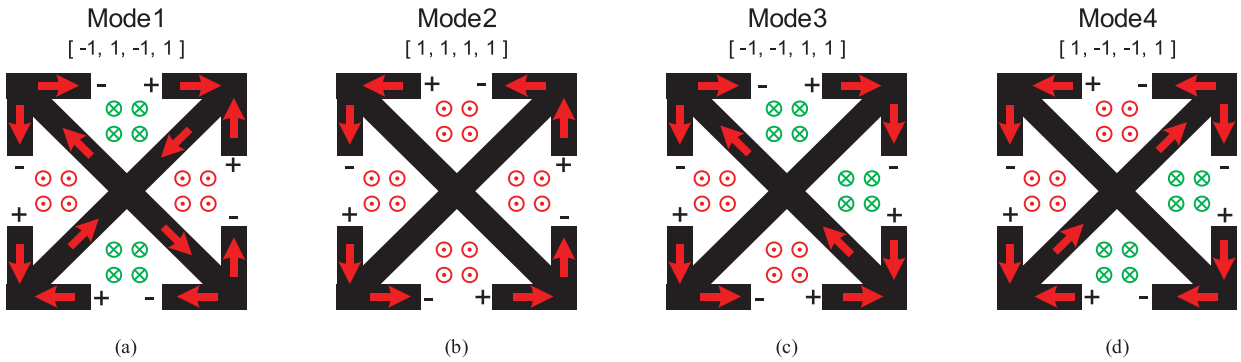


Fig. 6. (a)–(d) Four possible oscillation modes of the quad-core VCO.

corresponding to v_1, v_2, v_3+v_4 and v_3-v_4, respectively. It is worth mentioning that mode 2 is exactly the operating pattern of circular geometry multi-core VCO as shown in Fig. 2(c). Based on the model in Fig. 5(b), the Z-matrix is given by

$$\begin{aligned} a &= z_{11} = 2\left(\frac{(R_S+Z_2)Z_2}{R_S+2Z_2}+Z_1\right) \\ b &= z_{12} = -\left(\frac{Z_2^2}{R_S+2Z_2}+Z_1\right) \\ c &= z_{13} = 0 \end{aligned} \tag{8}$$

where $Z_1 = j\omega L_1$ and $Z_2 = j\omega L_2$. Substitute (8) to (6)

$$\begin{aligned} \lambda_1 &= j\omega\frac{\left(8\omega^2L_2^2+2R_S^2\right)(2L_1+L_2)}{R_S^2+4\omega^2L_2^2} \\ \lambda_2 &= \frac{4R_S\omega^2L_2^2}{R_S^2+4\omega^2L_2^2}+j\omega\frac{2R_S^2L_2}{R_S^2+4\omega^2L_2^2} \\ \lambda_3 &= \lambda_4 \\ &= \frac{2R_S\omega^2L_2^2}{R_S^2+4\omega^2L_2^2}+j\omega\frac{4\omega^2{L_2}^2(2L_1+L_2)+2R_S^2(L_1+L_2)}{R_S^2+4\omega^2L_2^2}. \end{aligned} \tag{9}$$

λ_1 is a pure reactance, which means R_S does not carry current at mode 1, while λ_2, λ_3, and λ_4 include both resistance and reactance and thus the Q-factor of the system at modes 2, 3, and 4 is degraded by the resistance term and these oscillation modes are suppressed by R_S.

The mode rejection can be analyzed by the equivalent quarter-circuit. A quad-core resonator is formed by the proposed inductor with each port connected by the same capacitor, as shown in Fig. 7(a). The quad-core resonator is symmetric in the x and y planes and the equivalent quarter-circuit can be simplified as shown in Fig. 7(b). The equivalent tank impedance is seen from each port Z_{in} is expressed as follows:

$$Z_{\text{in}} = \frac{\left(4L_1L_2C+2L_2^2C\right)s^3+(L_1+L_2)s}{\left(8L_1L_2C^2+4L_2^2C^2\right)s^4+4(L_1+L_2)Cs^2+1}. \tag{10}$$

The denominator of Z_{in} is a fourth-order polynomial, which implies two different conjugate pole pairs and thus two different resonant peaks. Fig. 7(c) plots the simulated Z_{in} of the resonator and shows that without mode ambiguity

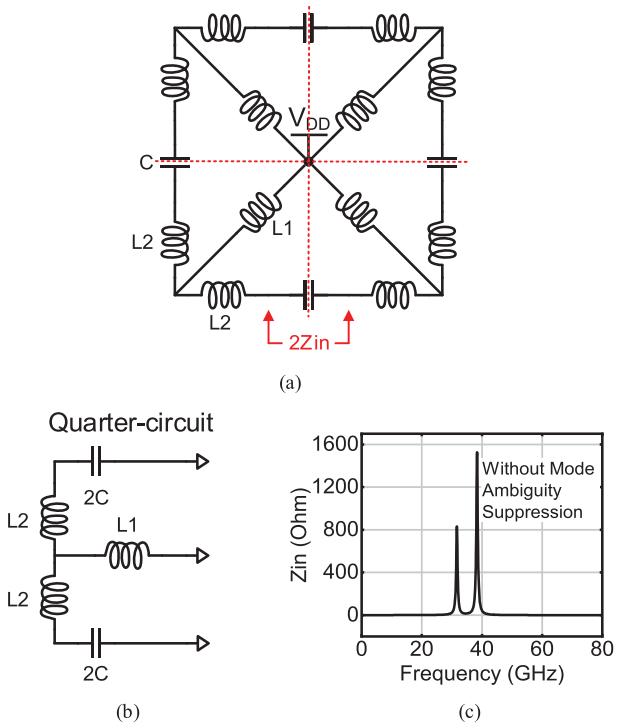


Fig. 7. (a) Proposed quad-core resonator without mode rejection resistor. (b) Equivalent quarter-circuit. (c) Simulated amplitude of Zin.

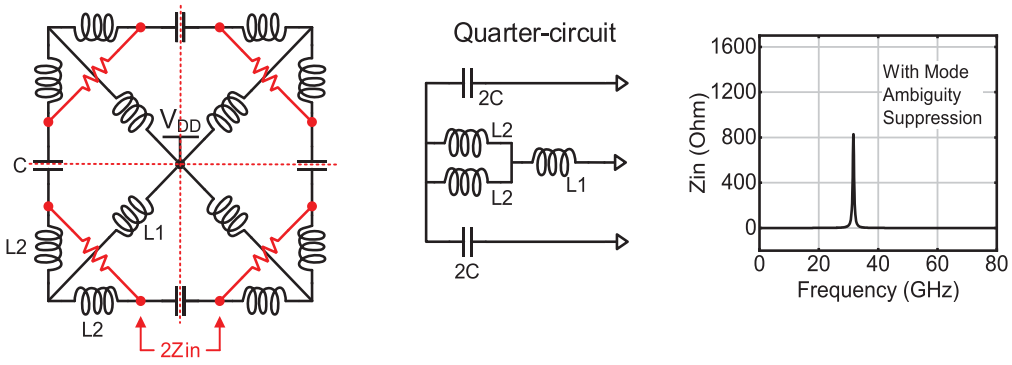
suppression, there are two oscillation peaks of Z_{in}. The oscillation frequency can be expressed as ω_{osc1} and ω_{osc2}

$$\omega_{\text{osc1}}^2 = \frac{1}{4\left(L_1+\frac{L_2}{2}\right)C} \tag{11}$$

$$\omega_{\text{osc2}}^2 = \frac{1}{2L_2C}. \tag{12}$$

ω_{osc1} and ω_{osc2} relate to modes 1 and 2 in Fig. 6, respectively, where mode 1 is the desired mode while mode 2 is the undesired mode.

Fig. 8(a) shows the proposed quad-core resonator with mode-rejection resistors. As analyzed before, the voltage across the two ports of R_s are in-phase. The equivalent quarter-circuit is simplified as shown in Fig. 8(b). Obviously, it can be further simplified to an inductor $(L_1+L_2/2)$ parallel with a



(a) (b) (c)

Fig. 8. (a) Proposed quad-core resonator with mode-rejection resistors. (b) Equivalent quarter-circuit. (c) Simulated amplitude of Zin.

capacitor C, which implies a first-order LC network and there is only one oscillation mode given as (11). Fig. 8(c) shows the simulated Z_{in} of the resonator and there is only one oscillation peak left with mode-rejection resistors.

C. Considerations of the Mode-Rejection Resistor R_s

Equation (12) is derived under the simplified condition that the voltage across the two ports of R_s are ideally in-phase therefore R_s is considered to be short. Adding a little more rigor, the actual equivalent quarter-circuit of Fig. 8(a) is shown in Fig. 9(a). The equivalent tank impedance Z_{in} seen from each port is expressed as follows:

$$Z_{\text{in}} = \frac{2R_sCL_2(2L_1+L_2)s^3+L_2(2L_1+L_2)s^2+R_s(L_1+L_2)s}{\left[2C(2L_1+L_2)s^2+1\right]\left(2R_sCL_2s^2+2L_2s+R_s\right)}. \tag{13}$$

Note that if $R_s \to \infty$, (13) is the same as (10) and there are two oscillation peaks, as shown in Fig. 9. (c). If $R_s \to 0$, the denominator of (13) will degrade to a second-order polynomial and the oscillation frequency is the same as (12), as shown in Fig. 9(b). The first factor of the denominator of Z_{in} results in an oscillation peak the same as (12) and its frequency and amplitude are irrelevant with R_s. The second factor of the denominator of Z_{in} indicates a second oscillation peak related to R_s. Fig. 9(d) shows the simulated amplitude of the desired mode and undesired mode with different R_s values. As long as $R_s < 100\ \Omega$, the amplitude of undesired mode is almost 0, which is the same as the case when $R_s = 0$, therefore the simplification in Fig. 8(b) is reasonable. In addition, a resistor within 100 Ω is easy to implement using a narrow metal trace. As R_s grows to $k\Omega$ range, R_s could no longer be considered short. The amplitude of the second oscillation peak grows with the increase of R_s while the frequency of the oscillation peak is unchanged.

A more specific value of R_s is given with a resort to the Q-factor of eigenvalues analyzed in Section III-B. Equation (9) shows the effective impedance of the system at the oscillation of four modes, where L_1 and L_2 are assumed as ideal inductors, which means the quality factor of L_1 and L_2 is $+\infty$, the quality factor of $\lambda_1 \sim \lambda_4$ can be calculated as follows:

$$\begin{aligned} Q_1 &= +\infty \\ Q_2 &= \frac{R_S}{2\omega L_2} \\ Q_{3,4} &= 2\omega(2L_1+L_2)\frac{1}{R_S} + \frac{(L_1+L_2)}{\omega L_2^2}R_S. \end{aligned} \tag{14}$$

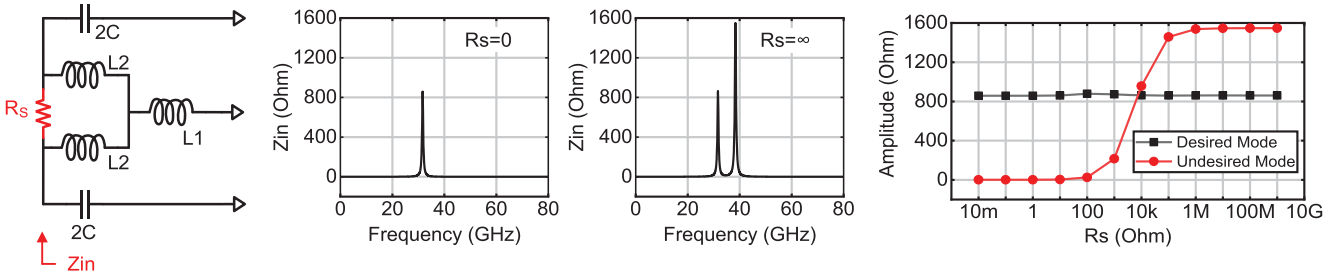
The mode rejection is achieved by degrading the Q-factor of the unwanted mode with R_S. Assumed that the series resistance of L_1 and L_2 is neglectable compared to R_S, the Q-factor of the desired mode Q_1 is $+\infty$, therefore, mode 1 is kept. The Q-factor of L_2 can be made arbitrarily small by reducing R_S thus mode 2 is suppressed. The Q-factor of modes 3 and 4 is non-monotonic with R_S and there is an optimum value of R_S which made $Q_{3,4}$ the smallest

$$R_{S,\text{opt}}^2 = \frac{2(2L_1+L_2)L_2^2}{(L_1+L_2)}\omega^2. \tag{15}$$

For example, if $L_1 = 70\ pH, L_2 = 30\ pH$, then $R_{S,\text{opt}} = 0.2\ \Omega$ at an oscillation frequency of about 20 GHz.

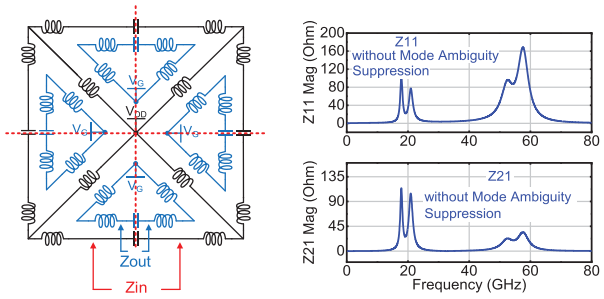
D. Class-F Operation

The proposed quad-core topology is convenient for various harmonic-shaping techniques. In this work, the class-F operation is adopted to pursue better PN performance. The schematic of the class-F resonation tank without mode-rejection resistors is shown in Fig. 10(a) with black inductors indicating the primary coils at drain nodes of transistors, while the blue inductors indicate the secondary coils at gate nodes of transistors. Fig. 10(b) shows the simulated Z_{11} and Z_{21}. The resonator shows a class-F characteristic with fundamental oscillation peaks at about 20 GHz and third-harmonic peaks at about 60 GHz. However, there are two peaks at both the fundamental and the third-harmonic frequency, which means mode ambiguity could happen. Fig. 11(a) shows the proposed quad-core class-F resonator with mode rejection resistor and the simulated Z_{11} and Z_{21} are shown in Fig. 11(b). With mode rejection resistors, the mode ambiguity is rejected and only one oscillation mode will be supported.



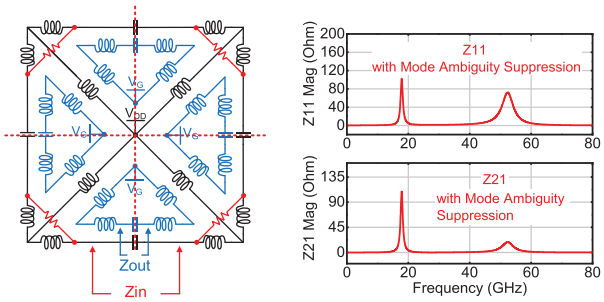
(a) (b) (c) (d)

Fig. 9. (a) Rigorous equivalent quarter-circuit of the proposed quad-core resonator with mode-rejection resistors. (b) Simulated amplitude of Zin with Rs = 0. (c) Simulated amplitude of Zin with Rs = ∞. (d) Amplitude of desired mode and undesired mode with different Rs values.



(a) (b)

Fig. 10. (a) Proposed quad-core class-F resonator without mode rejection resistor. (b) Simulated Z_{11} and Z_{21}.



(a) (b)

Fig. 11. (a) Proposed quad-core class-F resonator with mode rejection resistor. (b) Simulated Z_{11} and Z_{21}.

IV. Circuit Implementation

The complete schematic of the proposed quad-core VCO and its equivalent single-core circuit are shown in Fig. 12. The active devices in each of the four cores are identical. The negative resistance is provided by a CMOS differential pair and the size of the core transistors in each VCO is 16 × 2 μm/60 nm. C_d and C_g represent the capacitor array at the drain node and the gate node respectively and both have a 30% capacitance variable range with a 3-bit thermal code for the fine-tuning and a 3-bit binary code for the coarse tuning. Besides, C_d and C_g in each core can be controlled independently. The output signal is drawn from the gate node of cross-coupled transistors and it is a sinusoidal signal according to the characteristic of class-F operation. A differential common-source amplifier with a resistance load serves as the output buffer to drive the output load. The VCO buffer is driven directly only by one of the VCO cores and the dummy buffers are not added in the other three cores. This benefits the tuning range due to less overall parasitic capacitance but introduces a small load mismatch among four cores, proximately a gate capacitor of VCO buffer. It is later proved by the measured result in Section V that this mismatch has a neglectable influence on PN.

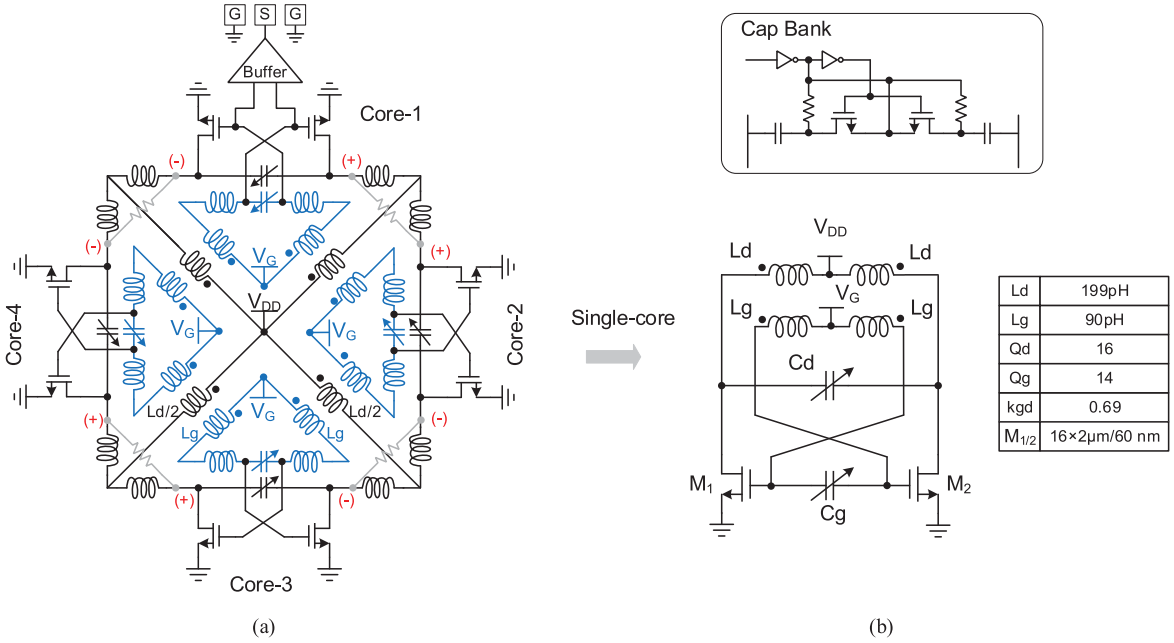
A. Square-Geometry Inductor Sharing Transformer

The layout of the proposed square-geometry inductor-sharing transformer is shown in Fig. 13(a). The coils at the drain L_d are implemented using the second-top metal layer M9 with a width of 20 μm, while the coils at the gate L_g are implemented using the third-top metal layer M8 with a width of 15 μm. The top metal layer is used for power supply routing. The four V_G bias nodes are connected together to the M6 layer and then connected to pads. M7 is used for mode-rejection metal trace resistor R_s. The spacing between the two coils is 3 μm to achieve the desired k_{gd}. Thanks to the square geometry and inductor sharing technique, the square-geometry transformer has a compact area of 0.252 × 0.252 mm^2.

Fig. 13(b) and (c) show the simulated results of the transformer, including the inductance, Q-factor, and mutual coupling coefficient. The results are extracted from the S-parameters generated by the EM simulator. The inductance of L_d and L_g at 20 GHz is 199 and 90 pH respectively, while the Q-factor of L_d and L_g at 20 GHz is 16 and 14 respectively. The coupling coefficient between L_d and L_g is around 0.69 over the operating frequency. Fig. 13(d) shows the simulated time-domain waveforms of the gate and drain voltages. The voltage at the gate and drain are sinusoidal and square-like, respectively, which verifies the class-F operation. Under a 0.9-V supply voltage, the max gate-oxide voltage is less than 1.8-V. According to the reliability analysis in [40] and [41], the lifetime due to time-dependent dielectric breakdown (TDDB) is longer than 40 years, which is sufficient for reliability considerations.

B. Potential Feasibility of Coupled VCO Array

The proposed square-geometry quad-core has the potential to expand to an even larger VCO array. As shown in Fig. 14, the square geometry makes it easy to be arranged in a compact matrix. The outputs of the neighbor core are close to each other which makes it easy to realize a tight coupling using a short and low-ohmic metal wire. Based on the proposed quad-core



Ld	199pH
Lg	90pH
Qd	16
Qg	14
kgd	0.69
$M_{1/2}$	16×2μm/60 nm

Fig. 12. (a) Detailed schematic of the proposed quad-core VCO. (b) Equivalent circuit of the single-core VCO.

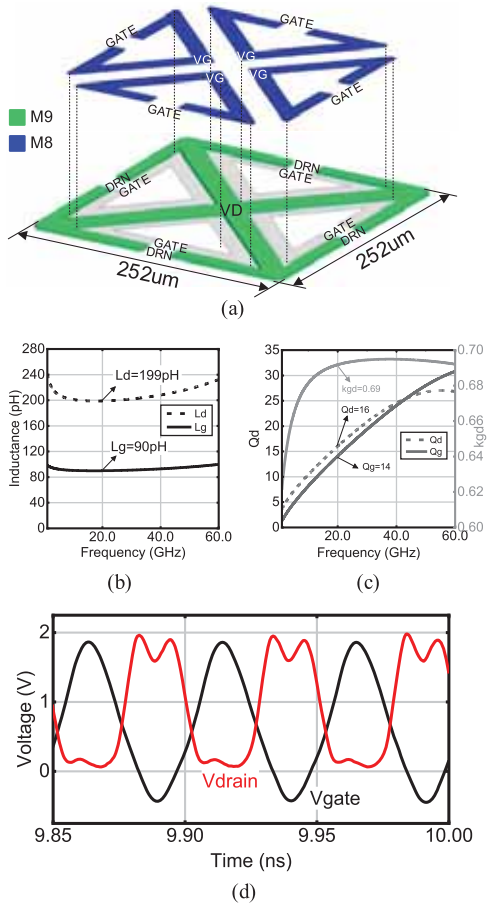


Fig. 13. (a) Top view of the square-geometry transformer. (b) and (c) simulated inductance, Q-factor, and coupling coefficient. (d) Simulated time-domain waveforms of gate and drain voltages.

VCO, one can realize 8-core VCO with a 1 × 2 matrix, 16-core VCO with a 2 × 2 matrix, and so on. As the circuit scale and

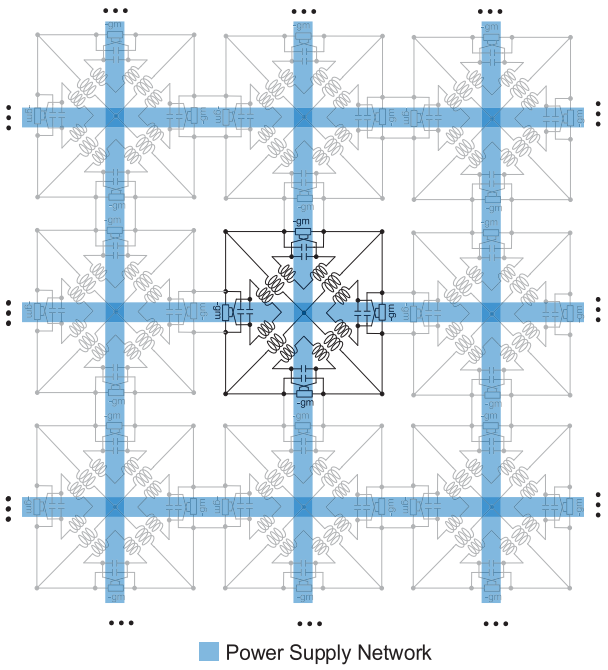


Fig. 14. Conceptual schematic of coupled VCO array.

chip area get larger, the oscillator cores in the middle are more susceptible to IR drop than the peripheral cores, therefore the power supply network should be paid more attention.

The inductor network at transistor gates is routing using the M8 layer, while the inductor network at transistor drains is routing using the M9 layer and both are in a 45° diagonal direction. The power supply network is implemented using top metal layer M10 to reduce IR drop and it is routed in a horizontal direction interweaved with a vertical direction to reduce the overlap with transformers, therefore reducing the

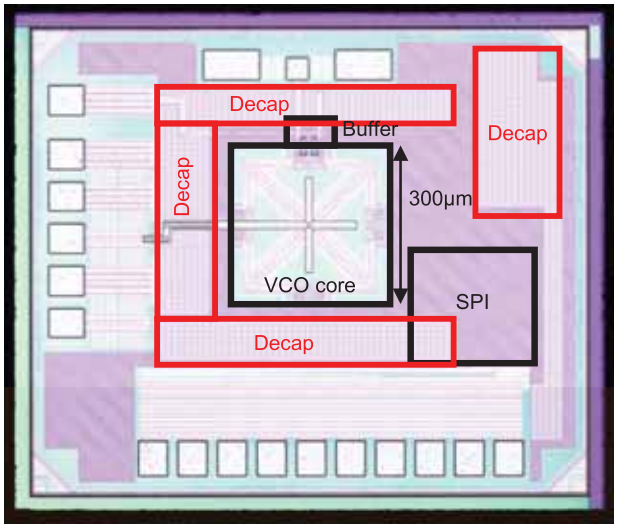


Fig. 15. Chip micrograph.

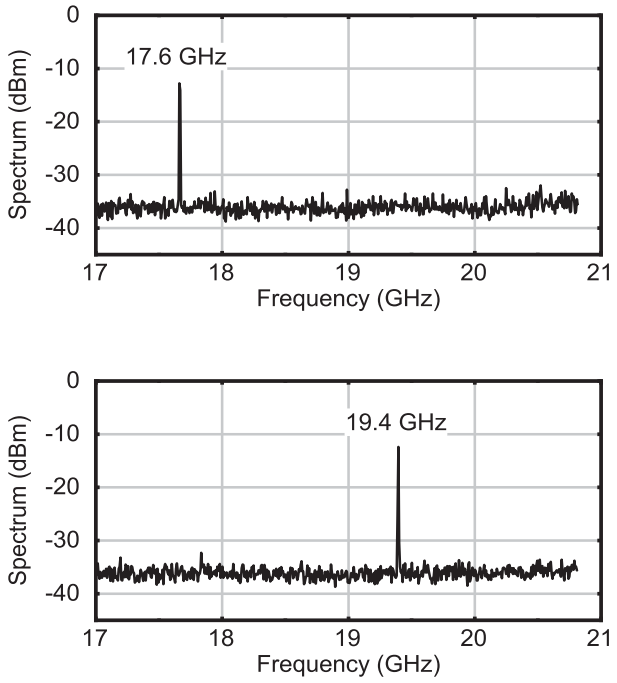


Fig. 16. Measured spectrum at minimum and maximum frequency.

coupling to the transformers and less affecting the Q-factor of the tanks.

V. Measured Results

The prototype of the proposed quad-core VCO was fabricated in a 65-nm CMOS process. The die micrograph is shown in Fig. 15. Thanks to the compact layout of the transformer, the core area of the VCO is 0.3×0.3 mm^2 excluding the output buffer and pads. The I/O signals are wire-bonded to a printed circuit board (PCB) for measurement. The output spectrum was measured using a Keysight E4440A spectrum analyzer and the PN performance was measured using an R and S FSWP50 PN Analyzer.

Fig. 16 shows the measured spectrum at the minimum and maximum frequency. The measured frequency-tuning range is about 2 GHz from 17.6 to 19.4 GHz. The output signal

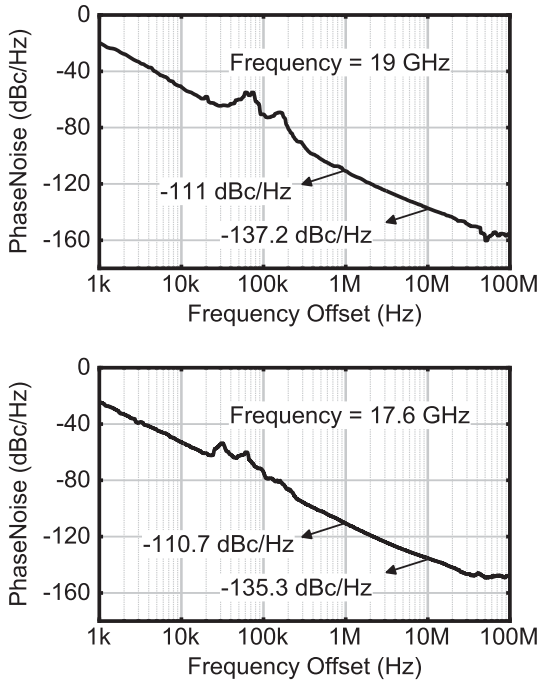


Fig. 17. Measured PN at 19 and 17.6 GHz.

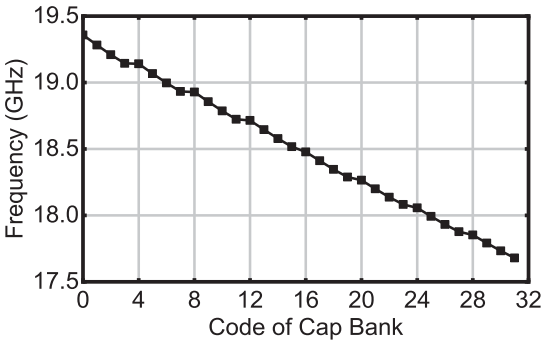


Fig. 18. Measured output frequency versus capacitor-bank settings.

is drawn from the gate node of cross-coupled transistors and it is a sinusoidal signal with a single spectral peak. Fig. 17 shows the measured PN of the proposed quad-core VCO. The measured PN is -111 dBc/Hz at 1 MHz offset and -137.2 dBc/Hz at 10 MHz frequency from the 19 GHz carrier frequency. It is noticed that there are bumps on the PN plot, which is believed to be caused by the power supply noise when the chip is tested on a PCB board. Under a 0.9-V supply voltage, the measured power consumption of the VCO is 46 mW and the corresponding figure of merit (FoM) at 10 MHz offset is 186.1 dBc/Hz. Fig. 18 shows the measured output frequency versus different capacitor-bank settings, where capacitor bank codes at the drain node and gate node are set identically and the capacitor-bank codes of four cores are also identical.

Fig. 19 shows the measured and simulated PN at 1 MHz and 10 offset over the whole frequency tuning range. The PN at 10 MHz offset varies from -137.2 to -135 dBc/Hz with about 2 dB variation. The corresponding FoM values are shown in Fig. 20, which vary from 182.2 to 186.1 dBc/Hz with less than 4 dB variation at a 10 MHz offset.

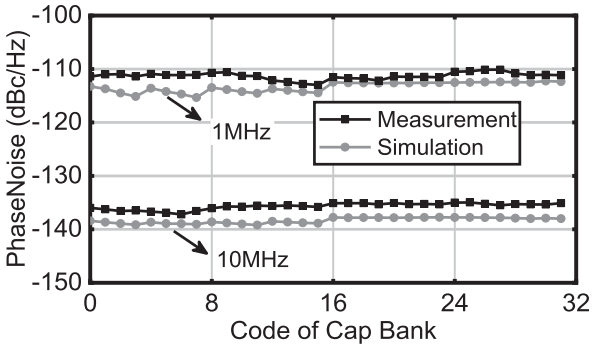


Fig. 19. Measured and simulated PN and at 1 and 10 MHz offset versus capacitor-bank settings.

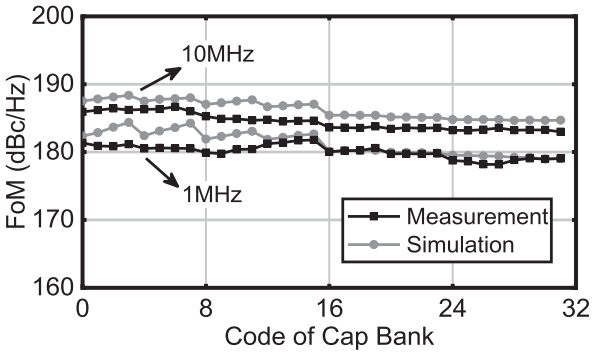
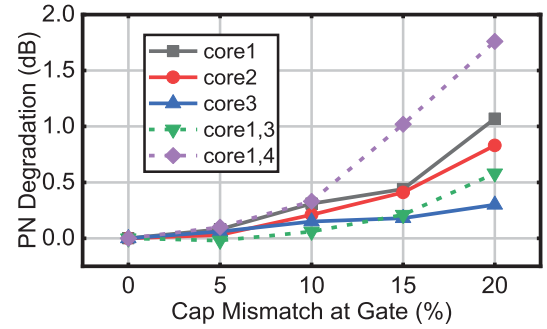
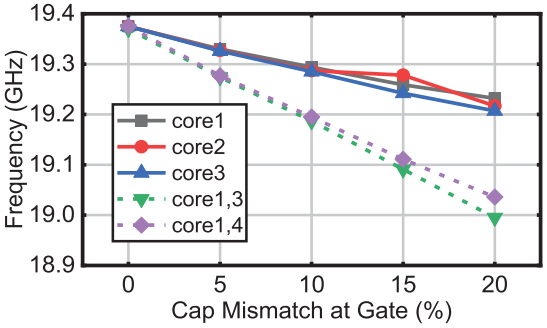


Fig. 20. Measured and simulated FoM at 1 and 10 MHz offset versus capacitor-bank settings.



(a)



(b)

Fig. 21. (a) Measured PN degradation at 10 MHz offset. (b) Oscillation frequency versus capacitor mismatch at gate added to different cores.

To verify the robustness of the proposed quad-core synchronization, the PN performance is measured with deliberate frequency mismatch added among four cores by setting different capacitor bank codes to the four cores.

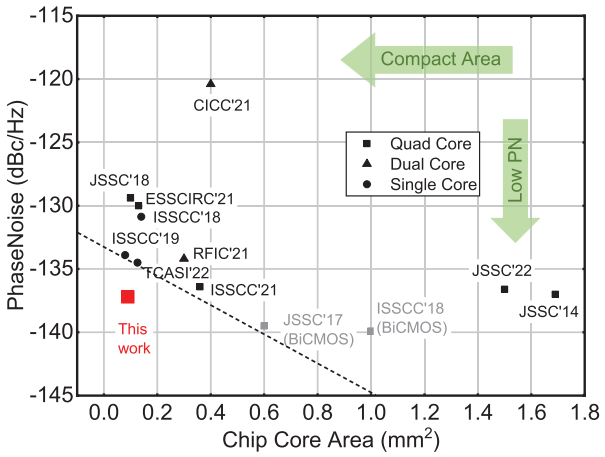


Fig. 22. Comparison of PN and chip area among state-of-the-art oscillators.

Core-1 is the core followed by the output buffer and core-1–core-4 are in the clockwise direction as shown in Fig. 11(a). Fig. 21 shows the measured PN degradation and frequency variation against the capacitor mismatch at the gate node added to different cores. The capacitor mismatch at the drain node is not considered because the capacitors at the gate node dominate the frequency. No locking loss is observed in the entire measurement. When the mismatch is added only to the core-1, the PN degradation is within 1 dB as the frequency mismatch increases to 20%. When the mismatch is added only to the core-3, the PN variation is less than 0.3 dB. When the mismatch is added to more than one core, the PN is a little worse but still less than 2 dB degradation. It is worthwhile mentioning that the mismatch caused by the input capacitance of the buffer is less than 2% thus the PN degradation due to the output buffer is neglectable, as claimed in Section IV.

Fig. 22 shows the PN performance and chip area comparison with prior arts which has a similar operating frequency, with PN normalizing to 19 GHz. To give a comprehensive comparison of PN and chip area, we select not only quad-core VCOs, but also dual-core and single-core VCOs. When compared to quad-core VCOs, which are represented by a square symbol in the figure, the proposed VCO shows the minimum chip area and a competitive PN performance. The two works represented by the gray square symbol show a better PN performance than the VCO we proposed because the process they use is BiCMOS [1], [16]. However, their chip area is six to ten times larger than the VCO we proposed. When compared to dual-core [11], [43] and single-core VCOs [38], [39], [40], [41], [42], which are represented by triangular and circle symbols, respectively, the proposed VCO shows an obvious better PN because there are more cores coupled together. Nevertheless, the chip area is not considerably larger, even smaller than some dual-core and single-core VCOs.

Table I summarizes more detailed measurement results and shows the comparison with the recently published multi-core VCOs with a similar operating frequency. The PN at 10 MHz offset is normalized to 19 GHz for a fair comparison.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH MULTI-CORE VCOS

	This work	ESSCIRC'21 [24]	JSSC'17 [1]	ISSCC'18 [16]	JSSC'18 [3]	JSSC'22 [22]	RFIC'21 [43]	TMTT'22 [12]
Technology	65nm COMS	65nm COMS	55nm BiCMOS	130nm BiCOMS	40nm CMOS	28nm CMOS	55nm BiCMOS	65nm CMOS
Number of Cores	4	4	4	4	4	2/4/8	2	2
Frequency [GHz]	17.6 to 19.4	17.9 to 20.7	17.5 to 20.2	11.8 to 15.6	23 to 29.9	10.7 to 14.1	18.9 to 22.6	8.2 to 21.7
Tuning Range [%]	10	16	15	15	26	27	16	89.3
PN @1MHz [dBc/Hz]	-111	-115	-118	-124	-110	-123[1]	-119.8	-100
PN @1MHz referred to 19GHz [dBc/Hz]	-111	-115	-117.9	-121.9	-112.4	-118	-120	-98.8
PN @10MHz [dBc/Hz]	-137.2	-130	-140	-142	-127	-141.6[2]	-134	-120
PN @10MHz referred to 19GHz [dBc/Hz]	-137.2	-130	-139.5	-139.9	-129.4	-136.6	-134.2	-120.4
Power [mW]	46	16.4	50	50	16	86.5	24	4
FoM @1MHz [dBc/Hz]	181	188.4	187.5	189	187	184	192	178
FoM @10MHz [dBc/Hz]	186.1	183.4	188	187	184	184	185.9	180
FoM_A @10MHz [dBc/Hz]	**196.5**	192.3	190.2	187	194	182.1	191.2	188
Core Area [mm^2]	0.09	0.13	0.6	1	0.1	1.55	0.3	0.4

$$\text{FoM} = |\text{PN}(\Delta f)| + 20log_{10}(f_0/\Delta f) - 10(P_{DC}/1mW)$$

$$\text{FoM}_A = \text{FoM} + 10log_{10}(1\text{mm}^2/Area)$$

[1][2]Estimated from PN plot with 4-core configuration.

The proposed VCO achieves the best PN in CMOS implementation and minimum chip area in quad-core VCOs with similar operating frequencies, resulting in an excellent FoM_A of 196.5 dBc/Hz.

VI. CONCLUSION

A 19-GHz quad-core VCO based on the square-geometry inductor-sharing transformer is presented. The inductor-sharing technique merges large inductors into smaller ones which greatly reduces the chip area. The quad-core VCO prototype implemented in a 65-nm CMOS process achieves a PN performance of −137.2 dBc/Hz at 10 MHz offset from a 19 GHz carrier, with a corresponding FoM of 186.1 dBc/Hz. Thanks to the compact layout of the transformer, the core area of the VCO is 0.3 × 0.3 mm^2 excluding the output buffer and pads, which is the smallest in quad-core VCOs with similar operating frequency and results in an excellent FoM_A of 196.5 dBc/Hz. In addition, the quad-core VCO has the potential to expand to a larger VCO array.

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